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RESEARCH ON SILICON SINGLE CRYSTAL THIN FILMS AND DEVICES

FIRST INTERIM
TECHNICAL REPORT
15 MARCH 1963

FIRST INTERIM TECHNICAL DOCUMENTARY REPORT FOR RESEARCH ON SILICON SINGLE CRYSTAL THIN FILMS AND DEVICES

by
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ABSTRACT

The purpose of this investigation is the acquisition of detailed understanding and control of the phenomena necessary to produce device-quality silicon films and silicon thin film diodes and transistors on an insulating polycrystalline substrate by hydrogen reduction of silicon tetrachloride. Deposition of device-quality silicon films on substrates coated with a mixture of oxides which are fluid at the deposition temperature is specifically investigated.

During this quarter various oxide mixtures were formulated and evaluated as fluid layers on the basis of light microscopy and electrical measurements of the silicon films deposited. Five formulations appear suitable for silicon film formation.

Silicon films formed at temperatures from 900° C to 1200° C were investigated by light microscopy for indications of preferred orientation; the results indicate that the optimum deposition temperature range is 1125° C to 1175° C. Films deposited in this temperature range were evaluated by resistivity and Hall effect measurements, from which hole and electron mobilities were calculated. The mobilities are about a factor of 10 lower than measured in silicon crystals grown by conventional techniques.

Evaluation of thin film silicon diodes and transistors was started.

SECTION I

PURPOSE

It is the purpose of this investigation to develop techniques for deposition of device quality silicon films on a polycrystalline substrate by hydrogen reduction of silicon tetrachloride vapor and to deposit thin film diodes and transistors for use in conjunction with passive thin film networks.

This program is an extension of work done as part of a Sylvania sponsored project which resulted in the rheotaxial approach (i.e. deposition of silicon on fluid layers).

The potential advantages of a capability to deposit thin film silicon diodes and transistors are increased reliability and reduced cost of thin film microcircuits. The improved reliability will result from elimination of man-made interconnections existing in present day thin film circuits using attached active components. The cost reduction will result from the decreased number of production steps required to produce a complete microcircuit.

The results of this research and development program will provide a knowledge of methods of depositing device quality silicon in thin film form (and confirming devices) on insulating substrates, such as those used in the construction of thin film microcircuits. The feasibility of the developed process and techniques will be shown by fabrication of experimental silicon thin film diodes and transistors.

SECTION 2

GENERAL FACTUAL DATA

2.1 PRESENT STATE-OF-ART IN DEPOSITION OF SEMICONDUCTOR FILMS FOR DEVICE FORMATION

The formation of semiconductor single crystal films has been investigated by a number of research groups and the results reported in the literature[1-4]. The described techniques include epitaxial growth of films on substrates of the same material as well as semiconductor films on single crystal insulating substrates (e.g., NaI, CaF, etc.) whose crystal structure closely matches that of the desired overgrowth. It is considered that for a desirable and economical technique the substrate must be low in cost, have desirable electrical insulating properties, high process temperature tolerance and other suitable physical properties. It is doubtful if a single crystal substrate can be obtained to meet all these demands. The use of a polycrystalline substrate appears to be the most promising approach.

2.2 RHEOTAXIAL APPROACH

Sylvania has developed a technique for deposition of semiconductor films on polycrystalline substrate which uses a "fluid substrate" surface. This condition permits arriving silicon atoms to arrange themselves into a form suitable for device formation.

A fluid substrate has no individual substrate grains and it permits high atomic surface mobility. This means that the first crystallite will determine the orientation of the resultant film. The fluid substrate may be regarded as a molten solid or a condensed gas. In either case there is a freedom of movement of molecules and yet the molecules are held together by their own forces of mutual attraction. The fluid layer limits the growth in one dimension in space; in the other two dimensions the limitation is the substrate area.

The deposition of a silicon film on a fluid layer is called the "rheotaxial" method and was developed by Sylvania Microelectronics Laboratory prior to the award of this contract. "Rheotaxial" comes from the Greek: rheos- flow, fluid; taxis – arrangement.

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1. R. Clang, B.W. Kippenham, IBM Journal of Rsch. & Dev. 4, 299 (1960).
2. F.C. Marinace, IBM Journal of Rsch. & Dev. 4, 248 (1960).
3. A. Mark, Journal ECS, 108, 880 (1961).
4. W.G. Spitzer & M. Tanenbaum, Journal of Applied Physics 32, 744 (1961).

2.3 PLAN OF THIS INVESTIGATION

This investigation will establish the optimum conditions for the deposition of device-quality silicon thin films on insulating substrates with the film properties necessary for diode and transistor action and process reproducibility for the fabrication of active components for thin film circuit application. The rheotaxial method will lend itself to the formation of active components on a substrate which is compatible with passive component formation. This concept will enhance the reliability of thin film circuits by reducing the number of man made connections as well as reducing the overall circuit cost. The results of this program will also include demonstration of feasibility of an all thin film circuit.

SECTION 3

DETAIL FACTUAL DATA

3.1 DESCRIPTION OF EQUIPMENT AND DEPOSITION PROCEDURE

The equipment designed and in operation for forming a thin film silicon deposit on a liquid layer is shown in Figure 3-1.

The critical parts of the deposition system are of quartz and stainless steel construction. Heat for the vapor decomposition of $SiCl_4$ is supplied by an RF generator. The system is enclosed and vented to ensure both cleanliness and safety. The complete system is of ball and joint connections sufficiently sealed to support a vacuum of 10 microns.

The substrate is placed on a graphite pedestal which is supported by a quartz rod into which is inserted a Pt-Pt Rd thermocouple. The thermocouple is positioned such that it monitors the temperature of the midpoint of the substrate wafer. The substrate-holding assembly is enclosed in a quartz deposition tube. At the start of a deposition run the system is flushed with nitrogen for a sufficient length of time to displace any ambient atmosphere admitted during the loading operation. The nitrogen entering the system passes through a molecular sieve trap at liquid nitrogen temperature to ensure dryness. Nitrogen is flushed through the by-pass system to the mixing chamber, on through the deposition tube, into the liquid nitrogen cold trap to the outlet. After the nitrogen flush, purified hydrogen gas is passed through the molecular sieve cold trap, through the by-pass and mixing chamber, to the deposition tube, and is burned off at the outlet. To deposit an undoped silicon film the purified hydrogen is passed through the silicon tetrachloride flask at a rate from 0.1CFH to 1.5CFH; however, 0.25CFH to 0.5CFH seems optimum. The hydrogen carrying the silicon tetrachloride vapors is then combined in the mixing chamber with a predetermined amount of hydrogen arriving through the by-pass section; the resultant mixture of H_2 and $SiCl_4$ reaches the substrate where the reduction reaction takes place. During deposition, the substrate is maintained at a temperature of 1075° C - 1150° C; the glassy layer of the substrate is fluid at this time.

Group III and Group V doping elements are provided by cylinders of hydrogen gas containing 1 ppm of borane and phosphine respectively. These doping gases are fed into the system through micrometer valves permitting a

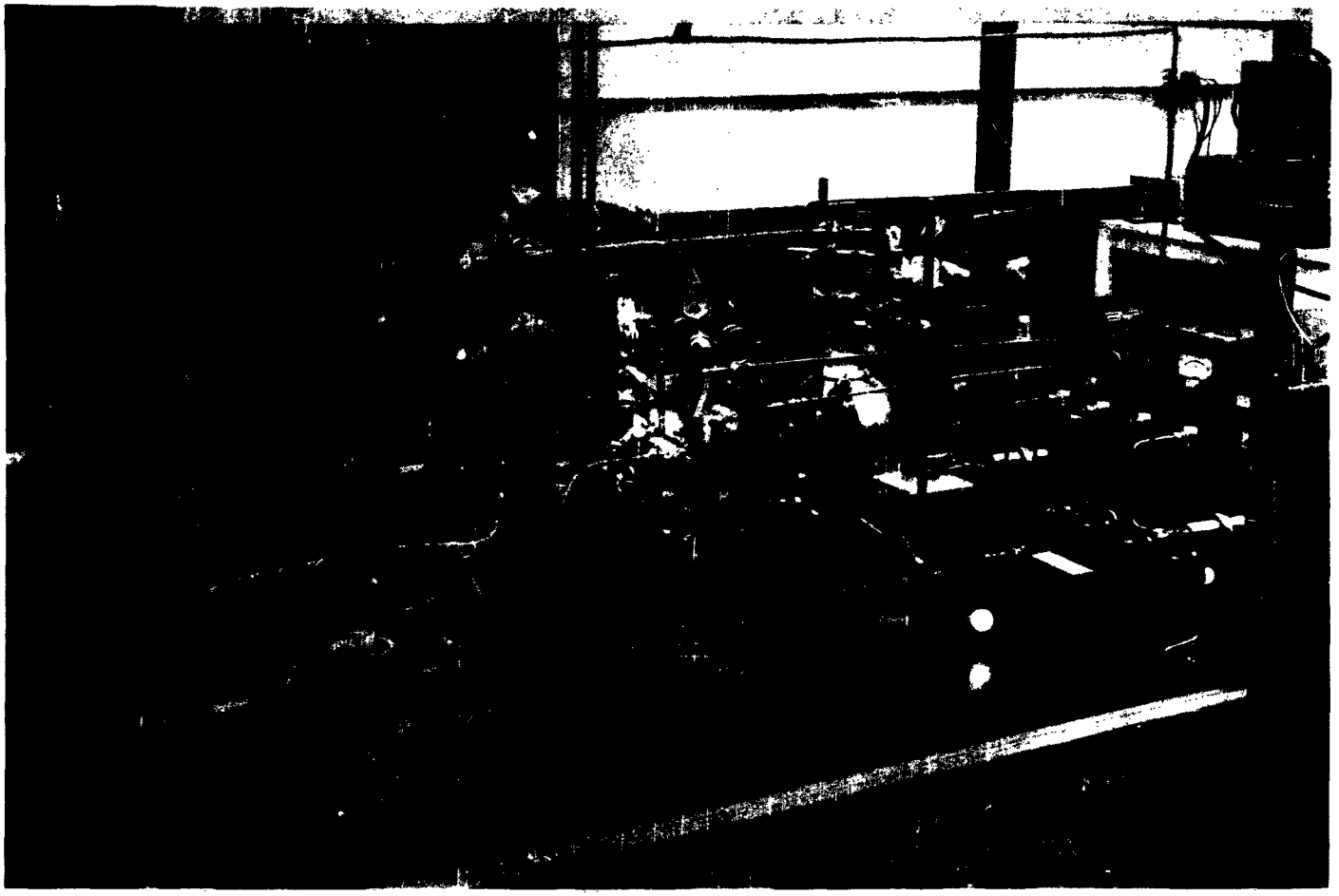


Figure 3-1. Apparatus for Silicon Deposition by Vapor Decomposition

high degree of reproducibility. The doping gases lead through separate lines to the mixing chamber and thence to the deposition tube. The valve settings of 0-25 on each doping line are calibrated and subsequent depositions with a specific valve setting will produce a specific n or p type film resistivity.

The silicon tetrachloride is of the highest purity available. It is sealed in quartz ampules against contamination when purchased and maintained contamination free throughout the experiments since it was established early in the program that the presence of any air or moisture during silicon deposition leads to various degrees of polycrystalline growth and non-continuous films.

3.2 CHEMISTRY OF THE SILICON DEPOSITION REACTION

The hydrogen reduction reaction of $SiCl_4$ temperatures is well known.[5] It occurs through the reversible disproportionation reaction, the forward

$$SiCl_4 + Si \rightleftharpoons 2\,SiCl_2$$

direction of which is increased by higher $SiCl_4$ vapor pressure and increased temperature. The reverse direction of this reaction accounts for the etching observed during depositions. The film growth itself must depend upon one or more of the species formed in the reduction of $SiCl_4$ by H_2; viz.,

$$2H_2 + SiCl_4 \rightleftharpoons Si + 4HCl$$

Intermediates such as $SiHCl_3$, SiH_2Cl_2, and SiH_2Cl will form,[6] as well as

$$SiCl_4 + H_2 \rightleftharpoons SiCl_3 + HCl + 1/2\,H_2$$

Free radicals could also be formed at or absorbed to the surface of the substrate and then be reduced further by gaseous species to atoms of silicon which result in silicon growth. To investigate the nature and rate of formation of the reduction products in order to verify one or more of the possible models would involve a complete study of the kinetics and mechanisms. A more pertinent study in this

5. H.C. Theurer, et. al., Proc. IRE 48, 1042 (1960).

6. E.S. Wajda, et. al., IBM Journal of Rsch. & Dev. 4, 288 (1960).

program is the formation of the glassy substrate layer, which is discussed in the next paragraphs.

3.3 FORMATION OF SUBSTRATE FLUID LAYER

The problem of finding a glass suitable for rheotaxial growth is threefold:

a) The glass must be made with the exclusion of all doping elements of silicon and elements that readily alloy with silicon.

b) The linear coefficient of thermal expansion of the glass should closely match that of silicon (i.e., 7.6×10^{-6} at 40° C).

c) The glass should be fluid at the deposition temperature.

The substrate for the glaze is a ceramic wafer (approximately 0.5" × 0.5" × 0.01") which has a coefficient of thermal expansion (6.5×10^{-6}) close to that of silicon. These wafers are thoroughly cleaned before the glaze is applied. The cleaning procedure is as follows:

1. 10 min hot trichloroethylene ultrasonically
2. 5 minutes demineralized water ultrasonically
3. 10 minutes 1:1 solution of HCl and HNO_3
4. 10 minutes demineralized water ultrasonically
5. 5 minutes demineralized water ultrasonically
6. 5 minutes methanol ultrasonically

After the cleaning process the wafers are air dried in a dust-free atmosphere.

It was determined that most commercially available glasses contain either a doping element as a major constituent or as an impurity. This fact necessitated the formulation of an acceptable glass from reagent grade materials in our own laboratory. By compounding raw materials to conform to the limitations of coefficient of expansion and softening point the following glazes were made:

NMS	Na_2O	15.4 percent
	MgO	10.0 percent
	SiO_2	74.6 percent

NMAS	Na_2O	15.75 percent
	SiO_2	74.4 percent
	MgO	8.6 percent
	Al_2O_3	1.75 percent
KMS	K_2O	19.2 percent
	SiO_2	72.6 percent
	MgO	8.2 percent
NMCS	Na_2O	18.0 percent
	MgO	3.9 percent
	CaO	5.4 percent
	SiO_2	72.7 percent
NCS	Na_2O	10 percent
	SiO_2	70 percent
	CaO	20 percent

The same general procedure was followed in formulating the above listed glass mixtures. The oxides, carbonates, or hydrates necessary to supply the proper composition were thoroughly ground by porcelain mortar and pestle to a particle size less than 300 mesh. It was determined that glazes for rheotaxial growth could not be ground by ball milling using stainless steel balls because the nickel impurities added to the glaze readily alloy with the silicon during deposition.

In all cases the glass mixtures contain either carbonates or water of hydration which is driven off with an initial firing at 800° C. The friable mixture remaining is reground to less than 300 mesh size and fired in a platinum crucible for fusion at about 1400° C in ambient atmosphere. In all cases the melt is reground and fired again at about 1400° C. In some cases additional firing steps are necessary to form homogenous glass.

The glass is now ground by mortar and pestle to less than 300 mesh size and mixed in a 1-1 ratio by weight with an organic binder, such as oil, which serves as a vehicle for the powdered glass and is driven off in subsequent baking. The silk screen method is used to apply the glass and oil mixture to the ceramic wafer. The silk screens are made by photolithographic techniques. The ceramic wafer is held on a jig below the silk screen. The mixture is

spread through the screen across the wafer to form a uniform layer. The wafer is placed on a hot plate to bake off the organic vehicle and allow the glass particles to settle uniformly on the surface of the wafer.

The final step is an empirical determination of the best temperature and time for fusing the glass to the wafer to form a smooth glaze. Experiments indicate a fusing temperature of 1300° C-1400° C to be acceptable.

All of the glaze compositions mentioned above are suitable for rheotaxial growth of silicon films. Results from more extensive electrical evaluation of the films deposited will lead to a choice of the preferred formulation.

3.4 RESULTS

During this quarter investigations were performed in the following areas:

1. Fluid layer formation
2. Substrate temperature optimization
3. Temperature gradient optimization
4. Effect of crystal growth rate.

The film depositions completed this quarter were evaluated through electrical measurement of properties of silicon films and pn junctions and metallography of surface structure of the films, the silicon film-glassy layer interface and the glassy layer-alumina substrate interface.

3.4.1 Metallographic Study of Silicon Thin Films

A Reichert Metallograph equipped for photomicrography and with magnification variable from 140 to 1600 diameters was the apparatus utilized in the metallographic evaluation. For photomicrography of minute details, a magnification of 1600 diameters was obtained with maximum extension of the camera bellows. Accessories employed in improving contrast and detail included polarizer, light filter, oblique light eliminator and interference contrastor.

Particular interests in the fluid layer include a possible interaction of this layer with the alumina substrate or the deposited film and the adhesion of the film to the fluid layer. The samples used to study these interfaces on

the metallograph were prepared by a cross-sectioning technique commonly used in the semiconductor field to determine junction depth in diffused pn junction devices. The units were bevel lapped at an angle of 5°, and cleaned in a dilute solution of hydrofluoric acid. The small angle used in this method provided maximum surface for examining the interfaces and the areas proximate to them for inclusions, decomposition or other signs of interaction. Figures 3-2a and 3-2b illustrate that this situation does not occur and Figures 3-3a and 3-3b indicate that this is true even for films which have a wrinkled appearance. The wrinkling, hence, is a condition caused not by a chemical decomposition of the fluid layer but by non-similar cooling rates. This condition is a result of an abnormally thick glaze, or failure of the glaze to completely cover the surface of the wafer. Also evidenced in these photomicrographs is the chemically insulating property of the fluid layer, as there is no obvious polycrystalline influence on the deposited film by the polycrystalline alumina substrate.

The intimacy of the silicon film's adhesion to the substrate was determined by etching a portion of the film away from the fluid layer. The surface of the glaze gave the appearance that the film had actually been impressed on the fluid layer. The impression in the glaze was very similar to the "orange peel" effect normally obtained after etching a silicon sample. Figures 3-4 and 3-5 indicate that this method can readily be used in determining the grain size and crystalline nature of the thin deposited films.

The surface structure of films deposited in experiments for obtaining substrate temperature, gradient optimization and the effects of growth rate, was evaluated for a variety of physical characteristics. These characteristics included film continuity, orientation, structure size, uniformity, site of nucleation and thickness.

The experiments in optimizing substrate temperature produced three critical temperature bands. The first of these exists below a temperature of 950° C where the films exhibit many intersecting lines of growth. These networks are probably formed by the intersection to twin growth paths. When two atoms meet and join together on the surface in a twined position they form a nucleation center for twin growth.[7] Since the mobility of these atoms is reduced

7. J.C. Courvoisier, L. Jansen, and W. Haidinger, "Two Dimensional Model for Crystallization from the Vapor Phase," 1962 Transactions, Amer. Vac. Soc.

Figure 3-2a. Polycrystalline Alumina Substrate - Glassy Layer (140X)

Figure 3-2b. Exploded View of Silicon Film Glassy Layer (1120X)

Figure 3-3a. Polycrystalline Alumina Substrate - Glassy Layer and Silicon Film Layer Interlaces (140X)

Figure 3-3b. Exploded View of Silicon Film - Glassy Layer Interlace (1120X)

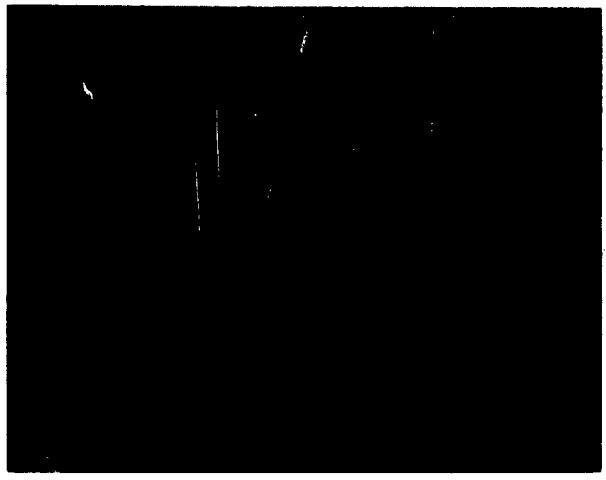


Figure 3-4. "Orange Peel" Effect Impressed on Glassy Layer (1120X)

Figure 3-5. "Orange Peel" Effect Showing Adhestion Properties (1120X)

on joining, the temperatures below 950° C probably reduce the mobility further, permitting a number of these nucleation areas to develop. Characteristic of these intersections is the angle of 60°, typical of twinned crystallization in films of (111) orientation. A series of these intersections are shown in Figure 3-6.

The mid-band extends from the 950° C temperature to 1150° C. In this region films for the most part exhibited a very similar, uniform structure and orientation, varying only with malfunction of the deposition system. Illustration of this normal type of film structure is seen in Figure 3-7.

Films deposited in the high temperature band, above 1150° C, were not continuous, exhibiting normal structure in a limited number of instances and then only at the center of the substrate. Beyond this, the films were quite obviously polycrystalline and eventually toward the perimeter there was only a random scattering of crystallites. It is expected that at these higher temperatures, the etching rate has begun to surpass that of the silicon deposition and above 1200° C, the effect is at maximum.

The temperature gradient of the substrate holder was adjusted to permit a 'cold spot' at or near the center of the substrate during deposition of the film. This 'cold spot' then becomes the center of nucleation for growth of the film. Nucleation is normally of two varieties, from a crystallite as pictured in Figure 3-8 or that of Figure 3-9 where the triangular (111) structure can be seen radiating from the nucleus.

An additional gradient arose when it became necessary to mask the border of the substrate to prevent wrinkling of the film in the cooling cycle. As a result of this new gradient, films appear as in Figure 3-10. The main body of the film exhibits normal film structure Figure 3- but enters into a polycrystalline transition area, Figure 3-11, then into a band about the perimeter of single crystalline appearance. This new gradient appears to provide the necessary conditions for initiating a film growth from the edges of the mask toward the center of the film, the polycrystalline transition area being the point at which the two directions of growth meet. The perimeter of single crystalline appearance in many instances show a triangular (111) type of orientation, Figure 3-12.

Figure 3-6. Networks Formed on Deposition η + 950°C (770X)

Figure 3-7. Normal Structure of Silicon Film (1120X)

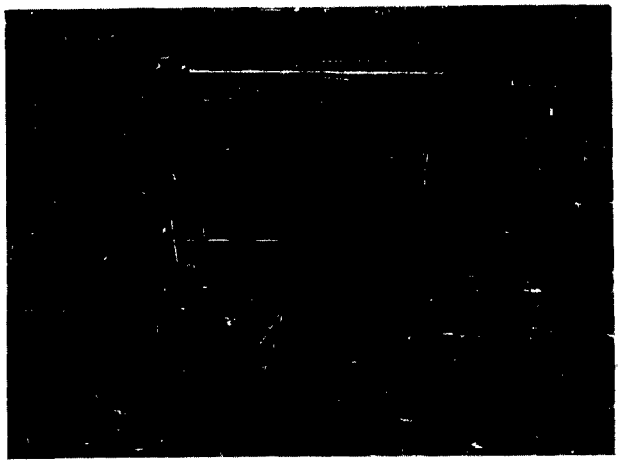


Figure 3-8. High Magnification of Crystallite Centered Nucleation (1120X)

Figure 3-9. High Magnification of Second Type of Nucleation, Indicating Triangular Order in Film Radiating From Nucleus (770X)

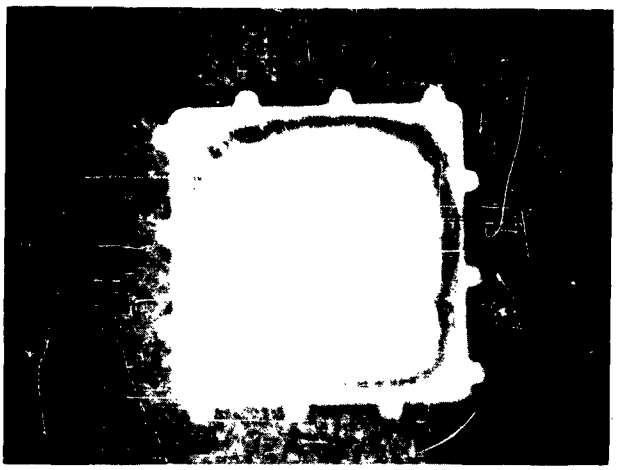


Figure 3-10. Silicon Film with Perimeter of Single Crystalline Appearance (10X)

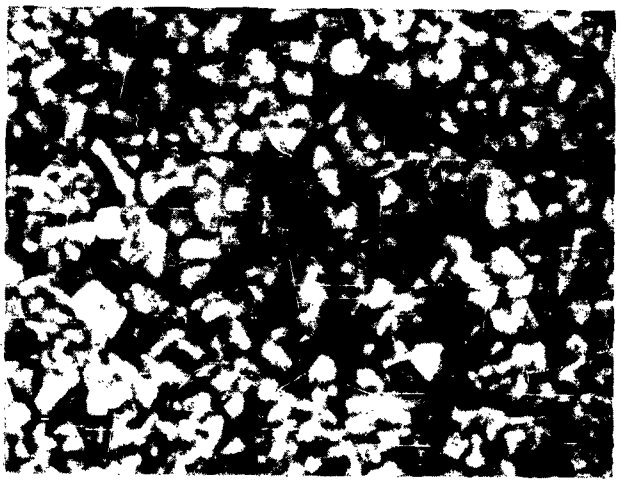


Figure 3-11. Polycrystalline Structure in Transition Area of Silicon Film (1120X)

Figure 3-12. Enlarged View of Area of Single-Crystalline Appearance (1120X)

In evaluating the films formed by varying growth rates, the thickness of the deposits was the only physical characteristic to change. Film thicknesses were measured on the metallograph by focusing first on the surface of the film and then on the glaze immediately along a sharp edge obtained through photolithographic and etching techniques. The thickness was the difference in the two focus settings on a vertical vernier calibrated at one micron/division. The films measured varied in thickness from 0.5 to 6 microns.

3.4.2 Electrical Study of Silicon Thin Films

The quality of silicon thin films deposited in the course of this program will be evaluated electrically through measurement of their bulk properties. The bulk parameters investigated were the conductivity type, resistivity, Hall effect and effective lifetime. A brief description of these techniques is given in the following sections.

3.4.2.1 Conductivity Type

Majority charge carriers, electroncs (n-type) or holes (p-type) can be readily determined in semiconductors by a hot-point probe. A hot metallic probe brought in contact with an n-type semiconductor creates electron-hole pairs near the probe.[8] Connecting the probe through a galvanometer to a cold contact at another location on the crystal will cause a current to flow to the hot probe as thermally produced holes are collected. Hence, the hot probe becomes positive in contact with n-type semiconductor and negative for p-type, in which thermally generated electrons flow to the probe.

The conductivity types for the films measured are included in Table 1. Group V elements (phosphorous, arsenic, antimony) as classified on the Periodic Chart of the Atoms are n-type doping elements.[9-11] Phosphorous in the form of phosphine gas, premixed with hydrogen, at the concentration of 1 P.P.M., is introduced into the reaction chamber during the deposition reaction to produce n-type silicon films. For p-type doping elements of Group III (boron, aluminum, gallium, etc.) are used. To produce p-type silicon films, borane gas was used instead of phosphine.

8. C.P. Hunter, Handbook of Semiconductor Electronics, Page 20-11.

9. J. Bardeen, W.H. Brattain, Phys. Rev. 74, 230, 1948.
10. W.H. Brattain, J. Bardeen, Phys. Rev. 74, 231, 1948.
11. J. Bardeen, W.H. Brattain, Phys. Rev. 75, 1208, 1949.

3.4.2.2 Resistivity

The conductivity of semiconductor materials is dependent upon the type of impurity present and the resistivity is determined by the concentration of that impurity. Two series of film depositions were completed when the concentration of p-type, borane dopant in one and n-type, phosphine dopant in the other, was varied. The resistivity of the films was measured by the four point probe method which for very thin films on non-conducting substrates is governed by the relationship:

$$\rho = \frac{\pi}{\ell n 2} \frac{V}{I} W$$

where

ρ = actual resistivity, Ω-cm

V = potential, volts

I = current, amperes

W = thickness, cm

The results of the resistivity measurements are shown in Figure 3-13 and in Table 1. In Figure 3-13 the resistivity of the n-type or p-type films changes as the amount of doping gas (phosphine or borane) is varied. The doping gas is controlled by the gauge settings; thus, the values of resistivity versus valve setting as pictured in Figure 3-13 may be plotted.

3.4.2.3 Hall Effect

The Hall effect is a phenomenon of semiconducting materials whereby a current flowing parallel to its length results in a potential along the axis normal to the current flow. When placed in a magnetic field (Figure 3-14) normal to the two axes, a transverse current flows as the field intensifies and the charge accumulates on the opposite faces until steady state is reached. The charge in potential occurring during this time is the Hall voltage. The sign of this increment is indicative of the film conductivity, n- or p-type. The Hall coefficient is given by:

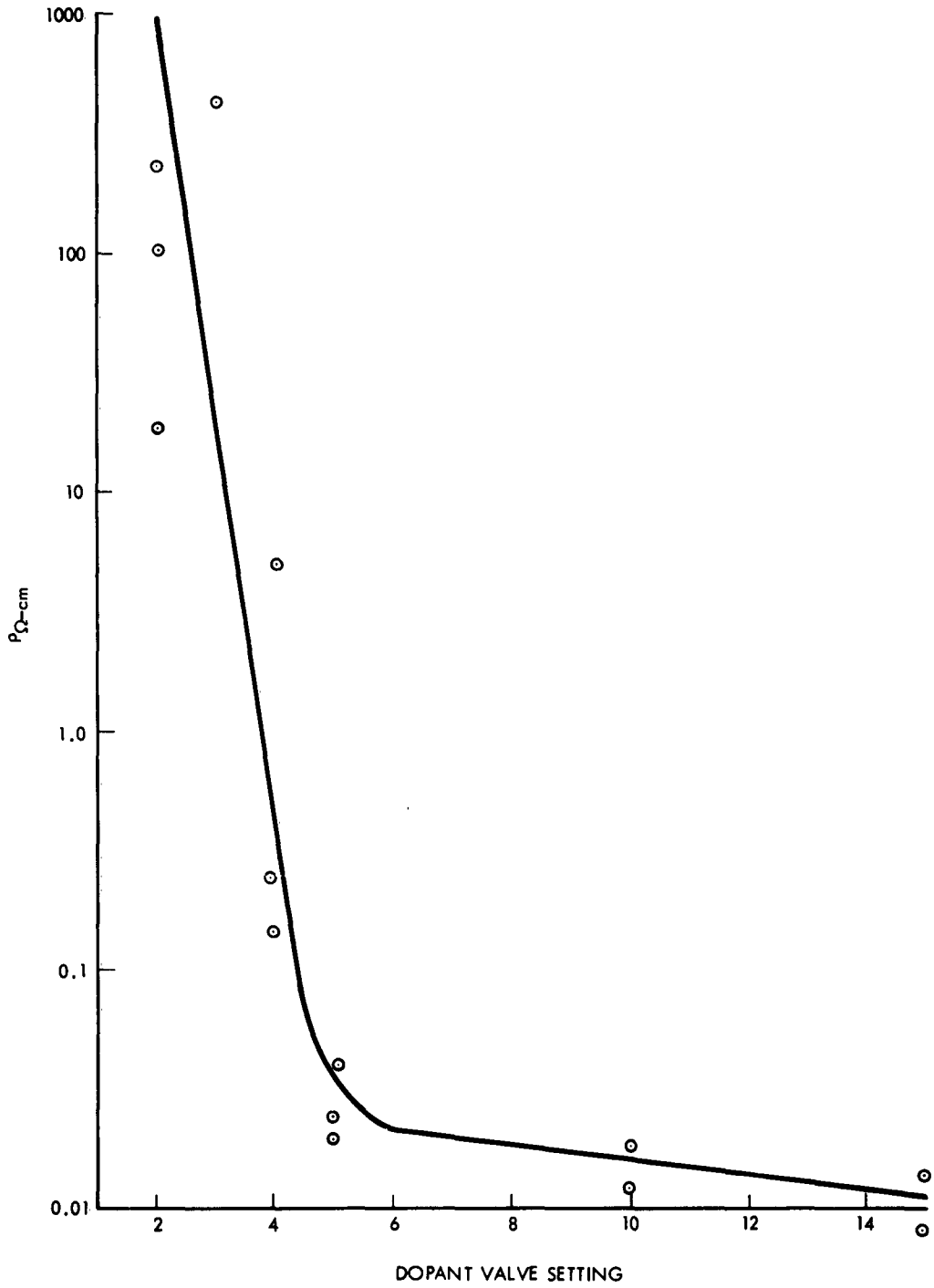


Figure 3-13. Resistivity of Pyrolytically Deposited Silicon Films Versus Vernier Valve Setting in Phosphine - Hydrogen Flow Line

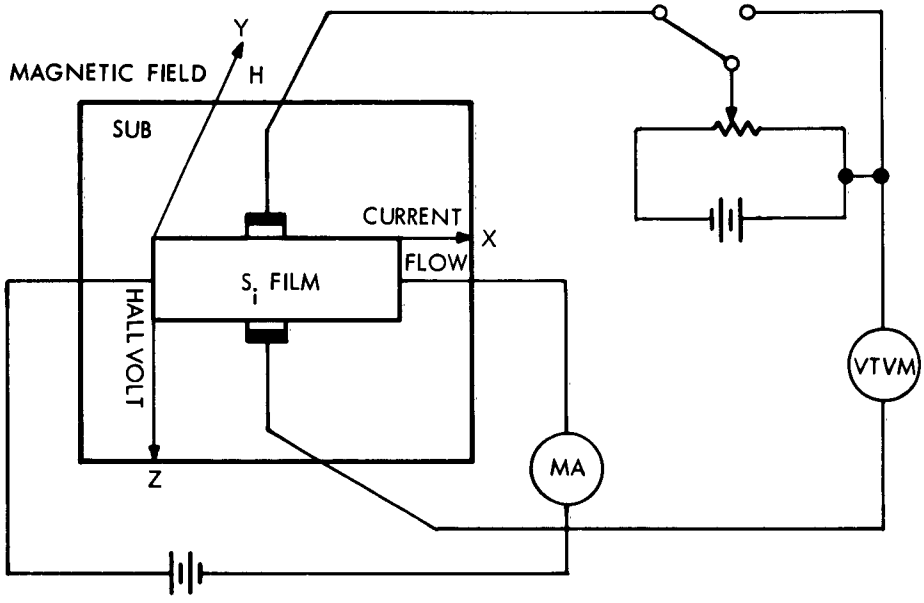


Figure 3-14. Silicon Film in Hall Pattern with Schematic of Electrical Measurement

$$R = 10^8 \frac{V}{I} \frac{W}{H}$$

where

R = Hall coefficient, cm^3/coulomb

V = Hall voltage, volts

I = current, amperes

W = sample thickness, cm

H = magnetic field, gauss

The coefficient 10^8 converts the electrostatic units to practical units. The Hall values, along with independent resistivity, yield the following electrical properties of the films:

A. The majority carrier density, N, obtained from R in the relation:

$$N = \pm \frac{3}{8} \frac{1}{Rq} \quad (+R - \text{p-type}, \ -R - \text{n-type})$$

where

q = electron charge

B. The mobility, μ, is obtained through a combination of Hall measurement and resistivity:

$$\mu = \frac{8}{3\pi} \frac{R}{\rho}$$

The values for Hall coefficient, majority carrier density and mobility of the films measured are presented in Table 1. The values of the mobility versus resistivity of n-type silicon as listed in Table 1 have been compared to data reported in the literature.[12] For example, the values reported by Morin and Maita are approximately a factor of 5-10 greater than the data reported in Table 1. This may be explained by the fact that thin film semiconductors in general are greatly influenced by surface effects. Thin film silicon devices will be treated to minimize this condition.

12. F.J. Morin, J.P. Maita, Phys. Rev. 96, 28 (1954).

3.4.2.4 Lifetime of Minority Carriers

A number of devices were made by the pyrolytic deposition techniques. Some measurements of these units were made to determine the lifetime of the material being produced.

The effective lifetime, T_e, of minority carriers was computed through change in diode conductivity. Carriers were injected into samples by electrical pulse, as shown in Figure 3-15, and the subsequent decay as the injected carriers recombined, was monitored on an oscilloscope. The measurement taken from the voltage decay is linear with time. The effective lifetime, T_e, is obtained from the relation:

$$T_e = \frac{kT}{q} \frac{\Delta t}{\Delta V}$$

where

T_e = effective lifetime, seconds

k = Boltzman's constant, 1.38×10^{-16} ergs/degree

T = temperature in degrees Kelvin

q = electron charge

Δt = increment of time after termination of pulse

ΔV = voltage change during Δt.

The lifetimes obtained for the units tested varied from 0.5 to 4 nanoseconds. These values are lower than those reported for bulk single crystals. For thin films, the surface lifetime can become controlling and mask any possible contribution of the bulk lifetime.

3.4.3 Diodes and Transistors

Devices have been fabricated throughout this portion of the program as a method of evaluating the quality of the silicon films. The rheotaxial deposition is made doping with either Group 111B elements or Group VB elements. Two techniques are used for the deposition of the second film for diodes and second and third film layer for transistors. In one method an oxide film is grown over the rheotaxial silicon deposit. By means of photolithographic techniques the

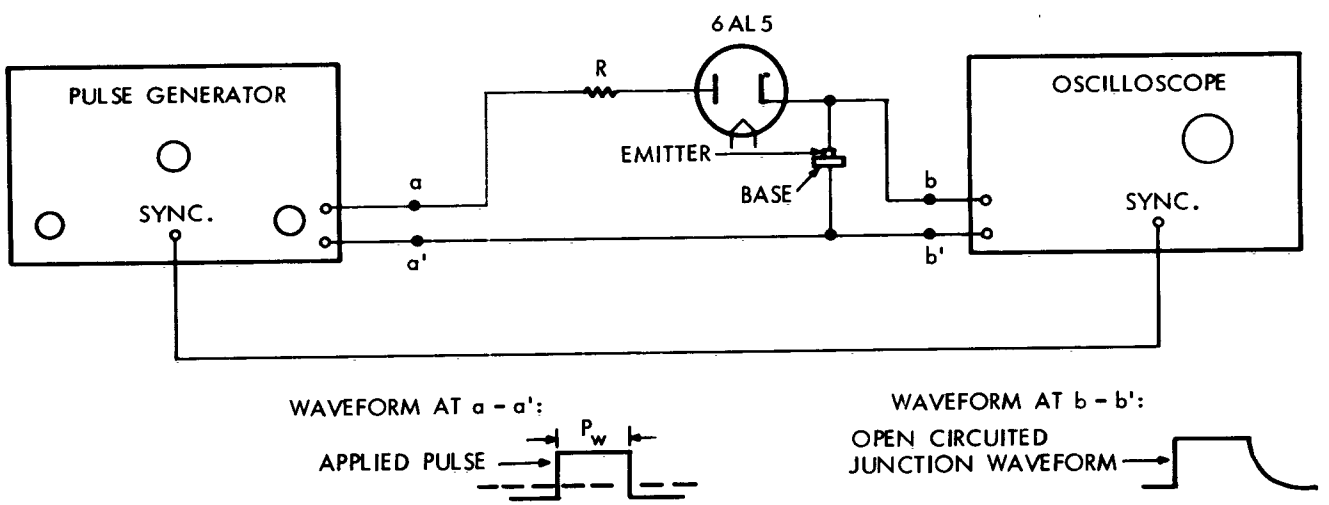


Figure 3-15. Minority Carrier Lifetime Circuit

oxide can be removed from specific areas and silicon deposited epitaxially onto these areas – the oxide masking against epitaxial growth elsewhere. This process may be repeated for successive depositions and making ohmic contacts.

In the second technique a silicon layer is deposited by the rheotaxial method doping with either Group 111B or Group VB elements. Without interrupting the deposition run or cooling the first deposition, successive films are grown epitaxially and doped during growth. The two or three layer device structure is masked and mesa etched as shown in Figure 3-16.

Contacts to the various regions of a diode or transistor structure are plated or vacuum evaporated through a photo resist mask, Figure 3-17.

Both techniques are being presently investigated. The first technique offers the advantage of providing the final structure for a diode or transistor where the junction areas are protected throughout the process by an oxide layer. The second technique offers the advantage that all depositions are performed in a single run and eliminates the need for photo-resist and chemical work between deposition steps.

Typical curve traces of diodes prepared by both techniques are shown in Figure 3-18, and Figure 3-19. The best diode reverse characteristics to date have been obtained by deposition thru oxide masks (Figure 3-18). Breakdown voltages in excess of 50 volts have been observed. The diode structures produced by mesa etching of films containing a pn junction have shown "soft" reverse characteristics. This is probably due to surface contamination which can be improved by surface passivation techniques.

Curve traces of silicon thin film transistors prepared by both techniques are shown in Figure 3-20 and Figure 3-21. The characteristics shown in Figure 3-20 were obtained from a transistor structure deposited through oxide masks. Since the oxide masks serves also as protection for the junction, the observed leakage currents are much smaller as compared to the "soft" characteristics shown in Figure 3-21 and obtained from a mesa transistor.

Surface treatments and various passivation techniques can likewise be employed to improve these transistor characteristics.

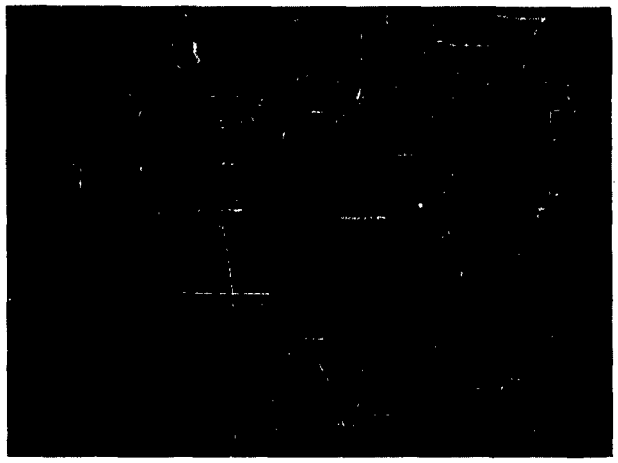
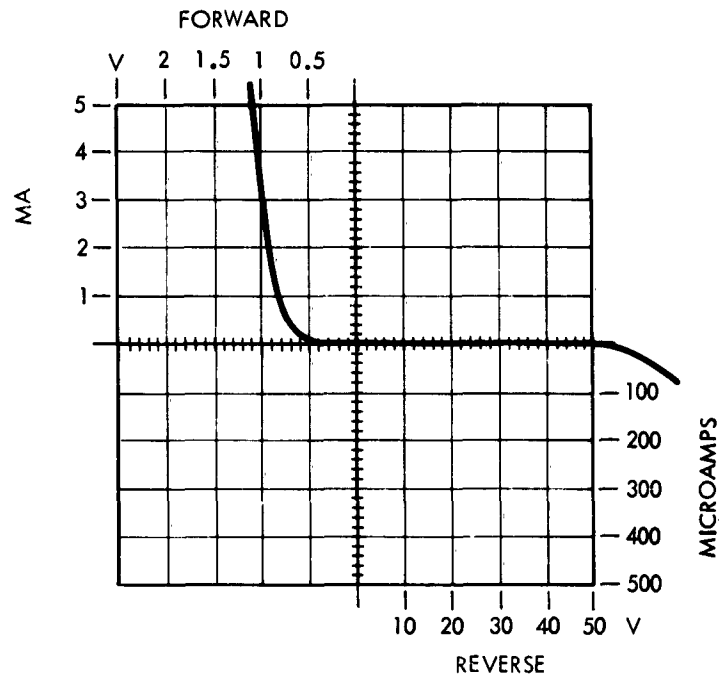


Figure 3-16. Etched Thin Film Transistor Structure

Figure 3-17. Etched Thin Film Transistor with Contacts (140X)



FORWARD CURRENT 3 MA AT 1V
REVERSE CURRENT (SAT. CUR.) 1 MICROAMP AT 50V

Figure 3-18. Characteristic of Thin Film Silicon Diode

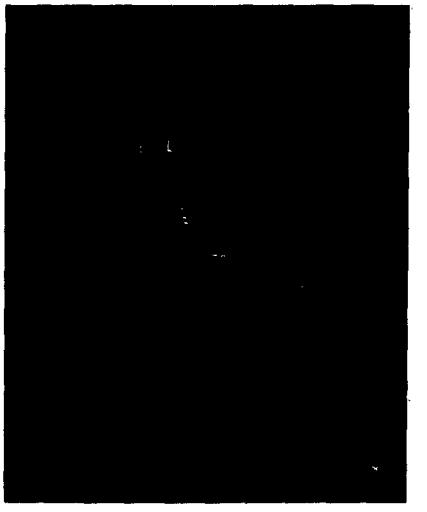
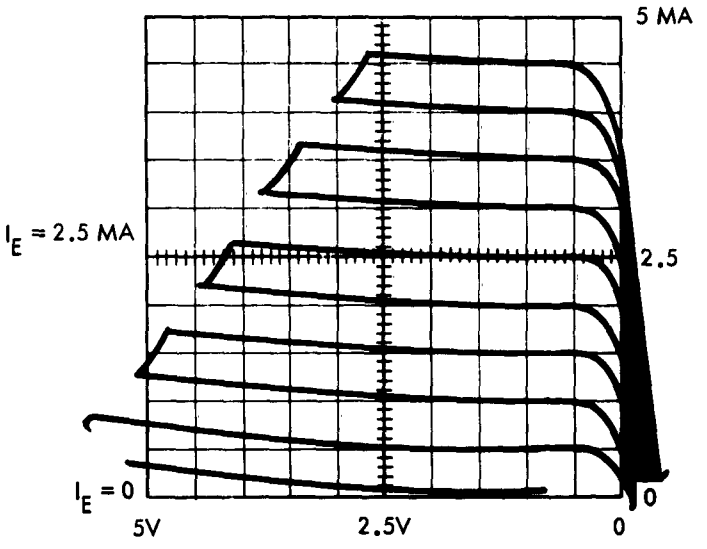


Figure 3-19. Forward and Reverse Characteristics of Thin Film "Mesa" Diode



ALPHA OF THIS TRANSISTOR = 0.985
GROUNDED EMITTER CURRENT GAIN (AT 5V = V_{CE} &
0.1 MA = I_B) = 60

Figure 3-20. Collector Characteristic of A SI Thin Film Transistor in the Grounded Base

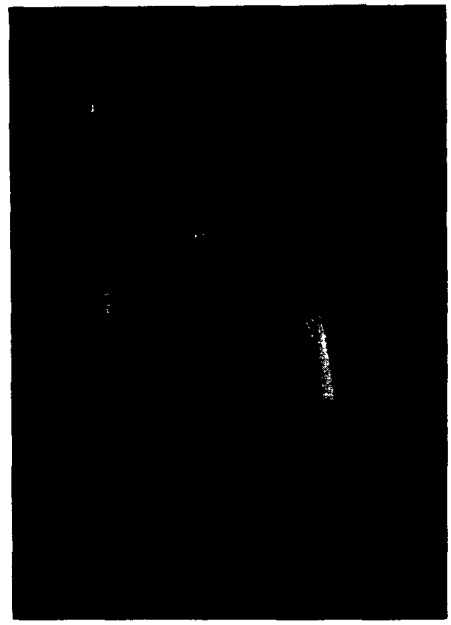


Figure 3-21. DC Characteristics of a Thin Film "Mesa" Transistor Grounded Base Configuration

3.5 PROJECT PERFORMANCE DATA

Figure 3-22 shows the schedule for completion of the various terms under the contract.

Listed below are the technical personnel working on this project.

Name	Title
E. Rasmanis	Project Engineer
R. Beatty	Engineering Specialist
G. Mannella	Engineering Manager
J. Madden	Senior Engineer
R. Hawks	Senior Technician
W. Brogan	Senior Technician
J. Nevers	Draftsman

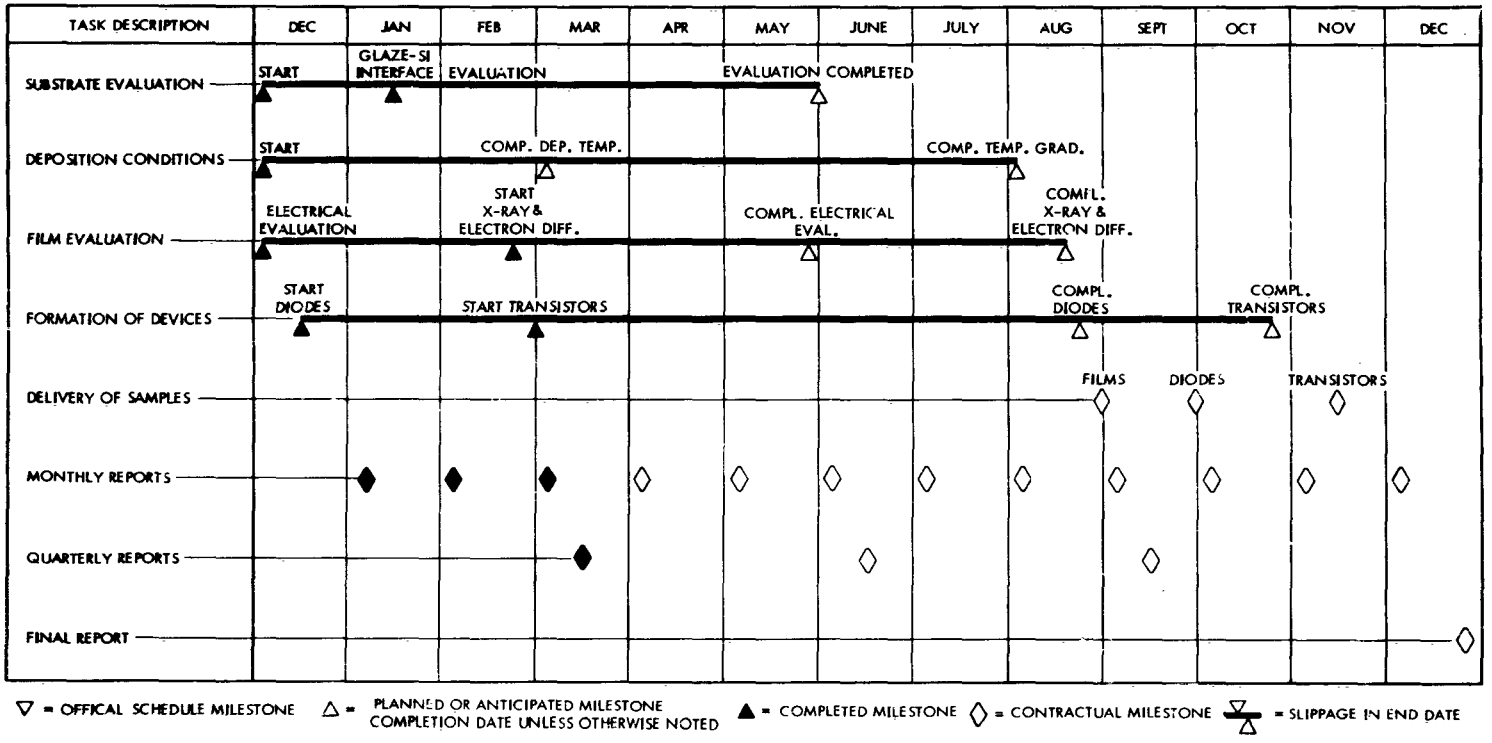


Figure 3-22. Engineering Schedule

SECTION 4

CONCLUSIONS

Deposition conditions have been investigated for growth rate control, substrate temperature optimization and temperature gradient optimization.

A number of glaze materials have been formulated and evaluated. Five glaze types are satisfactory for this phase of the program.

N-type and P-type silicon films have been deposited and evaluated optically and electrically. Diodes and transistors were fabricated by both oxide masking and etching mesa structures as a part of the silicon film evaluation studies.

PART II

SECTION 1

PLAN FOR NEXT QUARTER

1.1 SILICON DEPOSITION

During the next quarter it is planned to define the temperature effects related to growth rate, resistivity and conductivity types. The calibration of the N-type and P-type doping systems will be completed.

1.2 ELECTRICAL MEASUREMENTS

It is planned to measure resistivity, conductivity type, the Hall constant and minority carrier lifetime of the silicon films deposited. Complete evaluations will be made of the electrical measurements of intrinsic films, N-type films and P-type films.

APPENDIX A

BIBLIOGRAPHICAL REFERENCES

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Sylvania Electric Products Inc.
Sylvania Electronic Systems – East, Waltham, Mass.
RESEARCH ON SILICON SINGLE CRYSTAL THIN FILMS AND DEVICES, First Interim Technical Report (Unclassified Title), 15 March 1963, 39 pp. incl. 22 illus. (Sylvania Report No. Q403-1) (Contract AF33(657)-10488), 3 December 1962 Unclassified

The purpose of this investigation is the acquisition of detailed understanding and control of the phenomena necessary to produce device-quality silicon films and silicon thin film diodes and transistors on an insulating polycrystalline substrate by hydrogen reduction of silicon tetrachloride. Deposition of device-quality silicon films on substrates coated with a mixture of oxides which are fluid at the deposition temperature is specifically investigated.

During this quarter various oxide mixtures were formulated and evaluated as fluid layers on the basis of light microscopy and electrical measurements of the silicon films deposited. Five formulations appear suitable for silicon film formation.

Silicon films formed at temperatures from 900° C to 1200° C were investigated by light microscopy for indications of

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1. Microelectronic Devices
   -- active
   -- passive
2. Microelectronic Techniques
   -- vapor deposition
   -- vapor decomposition
3. Crystal Growth

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preferred orientation; the results indicate that the optimum deposition temperature range is 1125° C to 1175° C. Films deposited in this temperature range were evaluated by resistivity and Hall effect measurements, from which hole and electron mobilities were calculated. The mobilities are about a factor of 10 lower than measured in silicon crystals grown by conventional techniques. Evaluation of thin film silicon diodes and transistors was started.		preferred orientation; the results indicate that the optimum deposition temperature range is 1125° C to 1175° C. Films deposited in this temperature range were evaluated by resistivity and Hall effect measurements, from which hole and electron mobilities were calculated. The mobilities are about a factor of 10 lower than measured in silicon crystals grown by conventional techniques. Evaluation of thin film silicon diodes and transistors was started.	
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